

REMARKS

Claims 1-3 and 7-22 are pending in the instant application. Claims 1, 7-12, 15, 17 and 20 are amended herein. No new matter has been added as a result of the amendments.

102 Rejection

Claims 1 and 3 are rejected under 35 U.S.C 102(e) as being anticipated by U.S. Patent No. 6,356,958 to Lin, hereafter referred to as Lin. The rejection is respectfully traversed for the following rational.

The Examiner is respectfully directed to amended independent Claim 1 which sets forth an embodiment of the present invention including:

a circuit comprising an analog circuit and a digital circuit wherein said analog circuit comprises a dedicated analog input and a dedicated analog output and said digital circuit comprises a dedicated digital input and a dedicated digital output;
a wirebond pad;
a processor; and
a user selectable switching circuit that selectively connects at least one of said dedicated analog input, said dedicated analog output, said dedicated digital input and said dedicated digital output to the wirebond pad under control of the processor after packaging of said circuit.

Claim 3 depends from Claim 1 and recites further features of the claimed invention.

Claim 1 has been amended to include the limitations "user selectable switching circuit" and "after packaging of said circuit." Lin fails to teach or suggest these limitations, as claimed.

Lin does not teach or suggest a microcontroller that includes a switching circuit and a wirebond pad wherein "at least one of said dedicated analog input, said dedicated analog output, said dedicated digital input and said dedicated digital output" are selectively connected by the switching circuit to the wirebond pad as is recited in Claim 1. In fact, Lin teaches away from the claimed embodiment by teaching in the Abstract, "the selectable functions are selected during packaging of the known good integrated circuit die."

This is very different from "a user selectable switching circuit that selectively connects at least one of said dedicated analog input, said dedicated analog output, said dedicated digital input and said dedicated digital output to the wirebond pad under control of the processor," as claimed. Lin purports to teach selecting the desired circuit functionality prior to packaging and the claimed invention selectively connects functionality at any time after packaging and is in fact, user selectable. Consequently, Lin fails to teach or suggest the embodiment of the Applicants' invention as set forth in Claim 1. As such, Claims 1 and 3 are not anticipated by Lin.

Applicants disagree with the Examiner that Lin teaches "a switching circuit that selectively connects at least one of said dedicated analog input, said dedicated analog output, said dedicated digital input and said dedicated digital output to the wirebond pad under control of the processor, or selectable by a user" as claimed. Lin may purport to teach selecting inputs and outputs prior to packaging, however, the circuit of Lin does not allow "user selectable" switching by the processor, after packaging, as claimed. As such, Claims 1 and 3 are patentable over Lin and are in condition for allowance. As such, Applicants respectfully solicit allowance of Claims 1 and 3 based on this rational and the amendments to Independent Claim 1.

103 Rejection

Claims 1, 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,509,758 to Piasecki et al., hereafter referred to as Piasecki in view of the reference, Wirebonding: Reinventing the process for MCMs by H.K. Charles, et al., hereafter referred to as Charles. Piasecki and the claimed invention are very different. Piasecki teaches in column 2 lines 24-27 "a pin interface which allows both analog and digital signals to be coupled to respective processing circuits, via a single I/O pin." This is very different from the claimed embodiment. The claimed embodiment comprises "a dedicated analog input, a dedicated analog output, a dedicated digital input and a dedicated digital output."

The claimed embodiment uses dedicated pins for analog input and analog output and dedicated pins for digital input and digital output. Piasecki uses a single pin for both digital and analog input, which teaches away from the claimed embodiment.

Charles fails to remedy the deficiencies of Piasecki. Charles may purport to teach a wirebonding pad, however, Charles fails to teach or suggest "a switching circuit that selectively connects at least one of said dedicated analog input, said dedicated analog output, said dedicated digital input and said dedicated digital output to the wirebond pad under control of the processor," as claimed. As such, Claim 1 is patentable over Piasecki in view of Charles. Therefore, Claim 1 is in condition for allowance and allowance of Claim 1 is earnestly solicited for this rational.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,734,334 to Hsieh., et al., hereafter referred to as Hsieh in view of Charles. The rejection is respectfully traversed for the following rational.

Applicants have reviewed the Hsieh reference and respectfully assert that Hsieh fails to teach or suggest the claim limitations of the present invention. Hsieh purports to teach a programmable port for crossbar switch. However, Hsieh fails to teach or suggest "a dedicated analog input, dedicated digital input, dedicated digital output and a dedicated analog output," as claimed.

In fact, Hsieh teaches away from the claimed limitations of the present invention by teaching in column 2, lines 30-32 "each port can be programmably configured to provide a separate signal path for either analog or digital data signals passing in or out of the switch array." This teaches away from dedicated inputs and outputs for the both digital and analog signals, as claimed. As such, Claim 1 is patentable over Hsieh.

Charles fails to remedy the deficiencies of Hsieh. Charles may purport to teach a wirebond pad, however, Charles fails to teach or suggest "a dedicated analog input, dedicated digital input, dedicated digital output and a dedicated analog output," as claimed. For this rational, Claim 1 is patentable over Hsieh in view of Charles. As such, Claim 1 is in condition and allowance of Claim 1 is earnestly solicited.

Claims 1 and 7-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of U.S. Patent No. 5,107,146 to El-Ayat, hereafter referred to as El-Ayat. The rejection is traversed for the following rational.

For the rational stated above for Claim 1, Lin fails to teach or suggest "a user selectable switching circuit that selectively connects at least one of said dedicated analog input, said dedicated analog output, said dedicated digital input and said dedicated digital output to the wirebond pad under control of the processor," as claimed. El-Ayat fails to remedy the deficiencies of Lin.

In fact, El-Ayat teaches away from the claimed embodiment by teaching in the abstract, "a user configurable interface for conversion of signals from analog to digital form and from digital form to analog form." This is significantly different from "user selectively connecting at least one of said dedicated analog input, said dedicated analog output, said dedicated digital input and said dedicated digital output to the wirebond pad under control of the processor," as claimed. Furthermore, the inputs and outputs of El-Ayat are not dedicated, as claimed. The inputs and outputs of El-Ayat are programmable. For this rational, Claims 1 and 7-22 are patentable over Lin in view of El-Ayat. As such, Claims 1 and 7-22 are in condition for allowance and allowance of Claims 1 and 7-22 is earnestly solicited.

Conclusion

In light of the above-listed remarks, the Applicants respectfully request allowance of the remaining Claims.

The Examiner is urged to contact the Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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